ML42*x* User Guide

Virtex-4 FX FPGA RocketIO Characterization Platform

UG087 (v1.3) May 30, 2008

XILINX®

P/N 0402349-02

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/28/05	1.0	Initial Xilinx release.
09/28/05	1.0.1	In “Package Contents” section, added SMA wrench and deleted NQSL board. Minor text edits for clarity.
11/06/06	1.1	Added “22. System ACE MPU Port” section. Miscellaneous typographical edits.
03/02/07	1.2	Added “Additional Documentation”section. Updated “Package Contents”section. Added “Additional Information” section.
02/06/08	1.2.1	Updated Legal disclaimer. Updated the link to the product page in “Additional Information.”
05/30/08	1.3	Added the ML421 reference designators in Table 2, page 13. Added the ML424 reference designators in Table 3, page 14. Corrected VTT RX LEFT and VTT RX RIGHT for the ML421 and ML423 in Table 3, page 14. Corrected labels for ML423 in Table 8, page 16. Corrected pins 29, 31, 33, and 35 for ML424 in Table 14, page 19. Corrected VCC for ML421, ML423, and ML424 in Table 16, page 21. Corrected pin 62 for ML423 and pins 30 and 32 for ML424 in Table 18, page 22. Corrected labels J115 through J118 for ML423 in Table 21, page 25. Corrected MPA00 and MPA04 for ML421, and MPA06 for ML423 in Table 23, page 30.

Table of Contents

Schedule of Tables

Preface: About This Guide

ML42x RocketIO Characterization Platform

About This Guide

This document describes the features and operation of the Virtex®-4 FX FPGA ML42*x* series of RocketIO™ characterization platforms.

Additional Documentation

Information about the Virtex-4 family of FPGAs at http://www.xilinx.com/virtex4 includes:

- Product highlights
- Data sheets
- User guides
- Application notes

Additional information is available from the data sheets and application notes from the component manufacturers.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support cae WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Typographical Conventions

This document uses the following conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents.	See the *Virtex-4 FPGA Configuration User Guide* for more information.
	Emphasis in text.	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex4

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Support Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-4 FPGA Data Sheet.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML42x RocketIO Characterization Platform

Package Contents

- Virtex®-4 FX FPGA RocketIO™ characterization platform (referred to as the ML42*x* platform)
- User guide
- SMA-to-SMA cable assemblies
  - Four 24-inch cables
  - Two 12-inch cables
- System ACE™ CompactFlash memory card
- RS-232 cable
- SuperClock module
- Power supply module
- Power supply brick
- SMA wrench

Note: Development tools and PC download cable are not included and must be ordered separately.

Additional Information

The ML42x product page contains the platform's current information, including:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-4 FPGA features and technology
- Demonstration hardware and software configuration files for the System ACE controller
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in PADS PCB format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the Internet for viewing and printing these files.)
- Additional documentation, errata, frequently asked questions, and the latest news
- Contents of the CompactFlash card provided with the ML42*x* platform

Related Documents

Prior to using the ML42*x* platforms, users should be familiar with Xilinx resources. See "References," page 30 for direct links to Xilinx documentation. See the following locations for additional documentation on Xilinx tools and solutions:

- EDK: www.xilinx.com/edk
- ISE® Design Suite: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Virtex-4 FPGAs: www.xilinx.com/virtex-4
- ChipScope™ Pro: www.xilinx.com/chipscope

Introduction

The ML42*x* platform allows designers to investigate and experiment with the features of RocketIO multi-gigabit transceivers (MGTs). This document describes the features and operation of the boards.

The platforms and their corresponding packages are shown in Table 1.

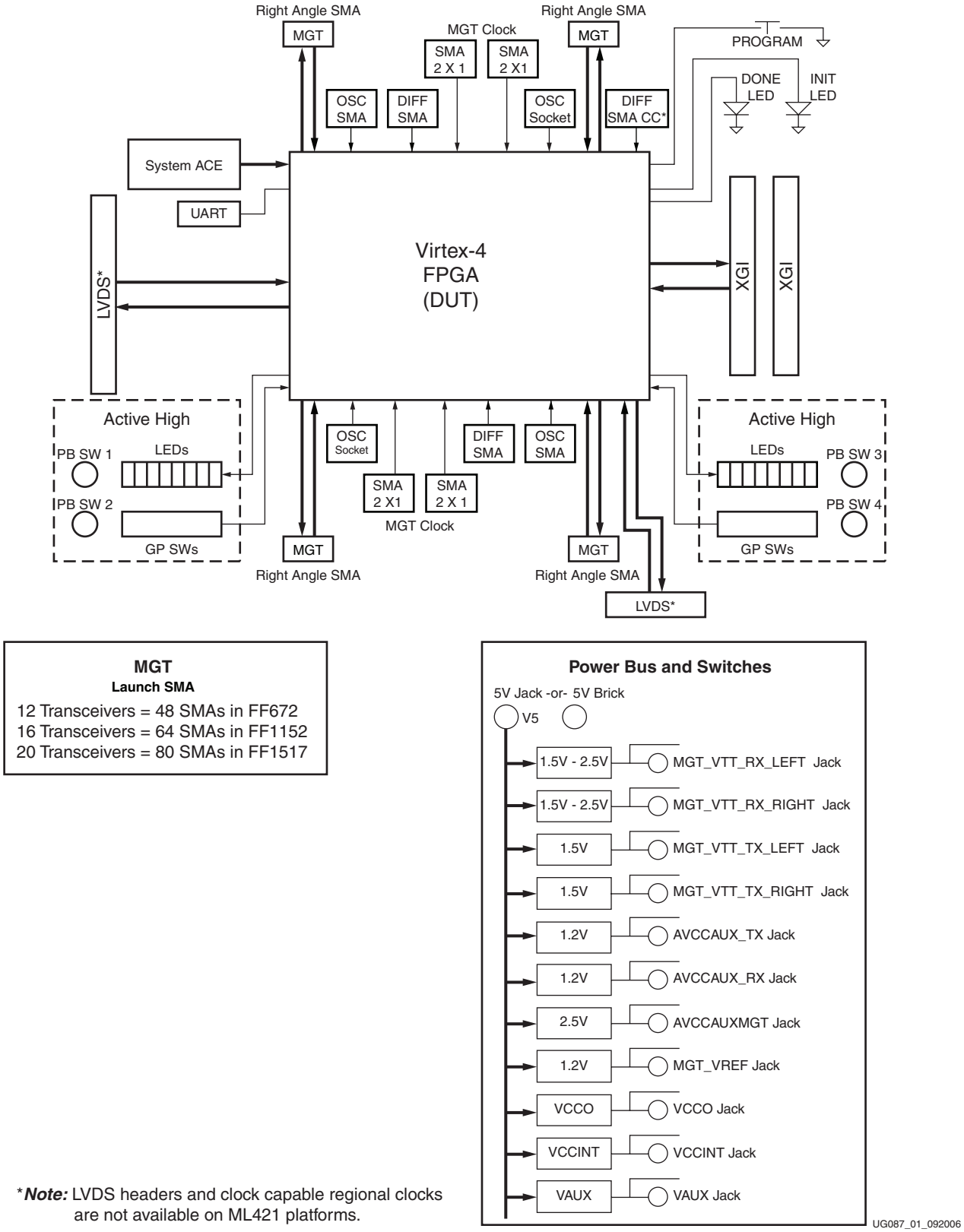
Table 1: **Platforms, Devices, and Packages**

Platform	Device	Package
ML421	XC4VFX60	FF672
ML423	XC4VFX100	FF1152
ML424	XC4VFX100	FF1517

Features

- Virtex-4 FPGA (referred to as the device under test, or DUT, in this user guide)
- Onboard power supplies for all necessary voltages capable of supplying 1.5A to 6A
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Parallel Cable III and Parallel Cable IV cables
- System ACE configuration controller
- RS-232 serial port
- MGT power supply module for supporting all transceiver power requirements
- Two 2.5V/3.3V global clock oscillator sockets
- Two single-ended global clock inputs with SMA connectors
- Two differential global clock inputs with SMA connectors
- Xilinx Generic Interface (XGI)
- SuperClock module with XGI
- 24 or 96 pairs of SMA connectors for the RocketIO transceivers
- Power indicator LEDs
- General purpose DIP switches, LEDs, and pushbutton switches
- One differential local clock input with SMAs
- Four differential MGT clock inputs with SMAs
- EU-RoHS-compliant

Figure 1 shows a block diagram of the board.



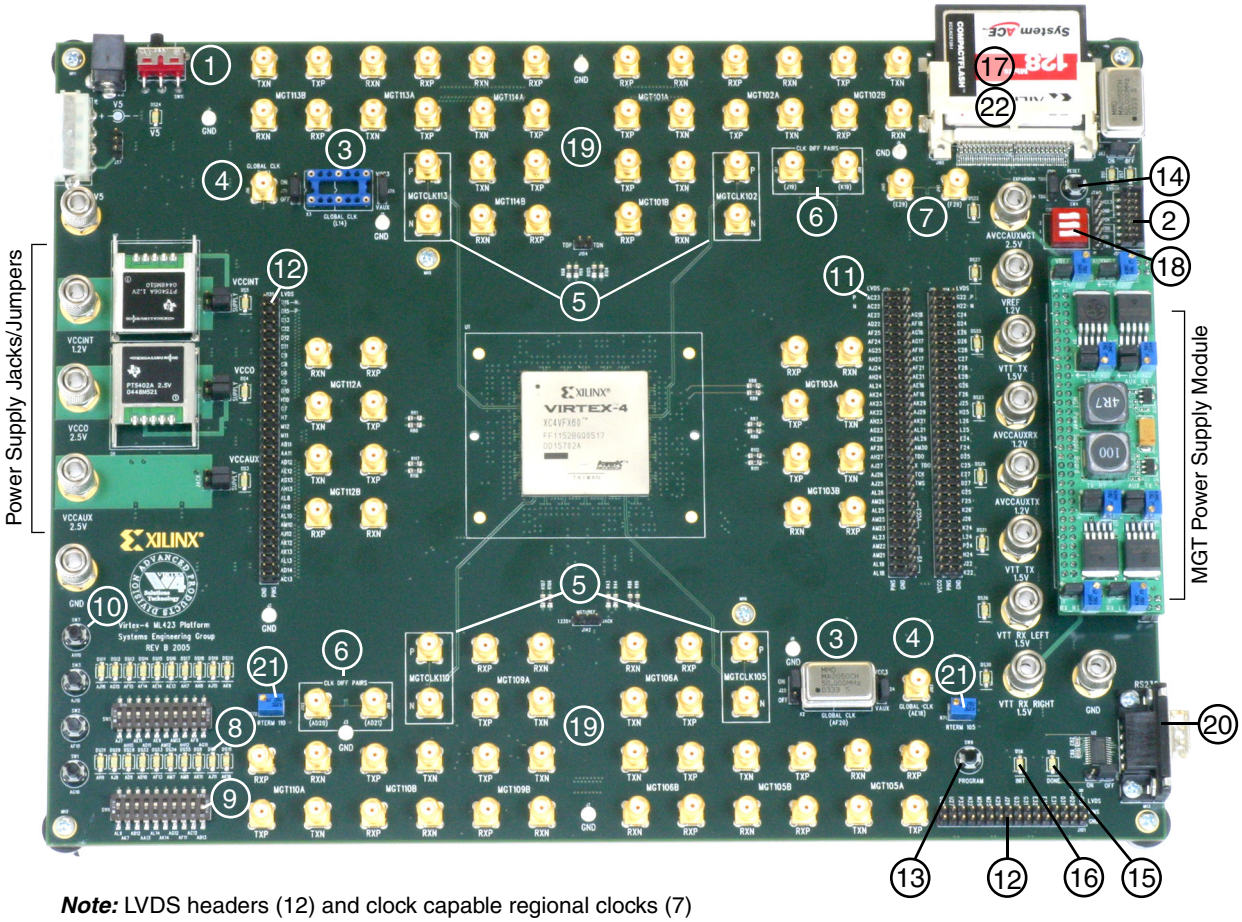
*Note: LVDS headers and clock capable regional clocks are not available on ML421 platforms.

Figure 1: **Virtex-4 FPGA ML42*x* Platform Block Diagram**

Detailed Description

The ML423 platform, shown in Figure 2, is an example of the ML42*x* series described in this user guide. Each feature is detailed in the numbered sections that follow.

Note: The image might not reflect the current revision of the board.



Note: LVDS headers (12) and clock capable regional clocks (7) are not available on ML421 platforms.

Figure 2: **Detailed Description of Virtex-4 FPGA ML42*x* Platform Components**

1. Power Switch

The board has onboard power supplies and an ON|OFF power switch. When lit, the V5 LED indicates power.

On Position

In the ON position, the power switch enables delivery of all power on the board by way of voltage regulators situated close to the left side of the board and the MGT power supply module situated close to the right side of the board. These regulators feed off the 5V external power brick or the 5V power supply jack.

The 5V power brick is capable of providing a maximum of 6.5A. For designs that require greater than 6.5A, an ATX power supply can be connected to the J16 hard drive power connector.

Note: 5V must always be supplied to the board to enable the 3.3V regulator for the System ACE chip.

Off Position

In the OFF position, the power switch disables all modes of power on the board.

Onboard Regulation

The ML42*x* platform has onboard regulation for the DUT main power supplies listed in Table 2. These regulators also have a corresponding input voltage jack to supply each voltage independently from the bench-top power supply.

Power Select Jumpers

The power select jumpers are labeled JACK on one side of the header and SUPPLY on the other side of the header. Appropriate placement of the jumpers on these headers enables delivery of power from either the onboard regulators or the corresponding power supply jack.

Table 2: **Onboard Regulation**

Power Supply Name	Max Current Rating	Typical Voltage	Jack			Description
			ML421	ML423 ML424	Select Jumper	
5V	N/A	5V	J9/J33	J27/J12	N/A	Main input voltage for the board supplied through the jack, barrel connector, or Molex connector
VCC3	3A	3.3V	N/A	N/A	N/A	Supplies 3.3V to the System ACE chip and other onboard circuits
VCCINT	6A	1.2V	J37	J34	J105	Core voltage for the FPGA
VCCO	6A	2.5V-3.3V	J34	J28	J106	I/O voltage for the FPGA
VCCAUX	3A	2.5V	J36	J33	J58	Auxiliary supply voltage for the FPGA

MGT Power Supply Module

The MGT power supply module supplies all voltages shown in Table 3 to the DUT RocketIO transceivers. This module plugs in on the right side of the board on header J12 for the ML421 platform, and on header J9 for the ML423 and ML424 platforms.

The onboard regulators also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply. This is done by removing the MGT power supply enable jumpers from the headers that correspond to each supply voltage listed in Table 3. An MGT power enable jumper must be removed before supplying an external supply on its corresponding supply jack.

Table 3: **Power Supply Module Jumpers**

Power Supply Name	Max Current Rating	Typical Voltage	Jack			Enable Jumper	Description
			ML421	ML423	ML424		
AVCCAUXMGT	1.5A	2.5V	J22	J22	J37	J11	Analog supply for global bias
VREF	1.5A	1.2V	J23	J23	J58	J10	Optional supply for V_{REF} circuit (not required) or band gap reference voltage
VTT TX LEFT	5A	1.5V	J19	J19	J24	J7 X 2	Termination supply voltage for transmitter A and B (left column)
AVCCAUXRX	5A	1.2V	J20	J20	J25	J5 X 2	Analog supply for non-I/O circuits in receiver A and analog supply for non-I/O circuits in receiver B, global bias, and reference clock circuits
AVCCAUXTX	5A	1.2V	J21	J21	J26	J4 X 2	Analog supply for non-I/O circuits in transmitter pair
VTT TX RIGHT	5A	1.5V	J18	J18	J18	J6 X 2	Termination supply voltage for transmitter A and B (right column)
VTT RX LEFT	1.5A	1.5V–2.5V	J16	J15	J15	J8	Termination supply voltage for receiver A and B (left column)
VTT RX RIGHT	1.5A	1.5V–2.5V	J105	J81	J105	J9	Termination supply voltage for receiver A and B (right column)

2. FPGA Configuration

The FPGA can only be configured in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- System ACE controller

Using the configuration address DIP switches, one of eight bitstreams stored in the CompactFlash memory card can be accessed through the onboard System ACE controller.

Note: The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, thus causing no disruption in the JTAG chain.

3. Oscillator Sockets

The ML42*x* platform has two crystal oscillator sockets, each wired for standard LVTTL-type oscillators. These connect to the FPGA clock pins shown in Table 4. The oscillator sockets accept both half and full sized oscillators and are powered by 3.3V or the V_{CCO} 2.5V power supply.

Table 4: **OSC Connections**

Label	Clock Name	Pin		
		ML421	ML423	ML424
X3	L8N_GC_LC_3	B12	L14	H18
X2	L5P_GC_LC_4	AB14	AF20	AK21

4. Single-Ended SMA Clocks

The ML42*x* platform has two single-ended clock input SMA connectors that allow connection to an external function generator. These connect to the FPGA clock pins as shown in Table 5.

Table 5: **SMA Clock Pin Connections**

Label	Clock Name	Pin		
		ML421	ML423	ML424
J96	L7N_GC_LC_3	A13	H18	J21
J103	L4P_GC_LC_4	AE13	AE18	AL20

5. Differential SMA MGT Clocks

The ML42*x* platform has four pairs of LVDS differential SMA MGT clock inputs as shown in Table 6. These are dedicated clock inputs for RocketIO transceivers.

Table 6: **Differential SMA MGT Clock Pin Connections**

Label	MGT Clock Name	Pin		
		ML421	ML423	ML424
J60	MGTCLK110_N	AF11	AP4	AW7
J61	MGTCLK110_P	AF10	AP3	AW6
J62	MGTCLK113_N	L1	K1	G1
J64	MGTCLK113_P	K1	J1	F1
J82	MGTCLK102_N	G26	N34	G39
J83	MGTCLK102_P	F26	M34	F39
J79	MGTCLK105_N	AF20	AP28	AW33
J80	MGTCLK105_P	AF21	AP29	AW34

6. Differential SMA Global Clocks

Two pairs of 100Ω differentially routed SMA connectors allow the user to connect to an external differential function generator. These connect to the global clock (GC) pins of the FPGA as shown in Table 7. These SMA connectors can also be used as single-ended clock inputs.

Table 7: **Differential SMA Global Clock Pin Connections**

Label	Clock Name	Pin		
		ML421	ML423	ML424
J97	L5N_GC_LC_3	B14	J19	L20
J98	L5P_GC_LC_3	C14	K19	L21
J102	L1N_GC_LC_4	AF15	AD20	AP21
J99	L1P_GC_LC_4	AE15	AD21	AP22

7. Differential SMA Regional Clocks

Two pairs of 100Ω differentially routed SMA connectors allow the user to connect to an external differential function generator. These connect to the *clock capable* (CC) regional clock pins of the FPGA as shown in Table 8. These SMAs can also be used as single-ended clock inputs.

Table 8: **Differential SMA Regional Clock Pin Connections**

Label			Clock Name	Pin		
ML421	ML423	ML424		ML421	ML423	ML424
	J140	J157	L8N_CC_LC_9		E29	H32
	J141	J156	L8P_CC_LC_9		F29	H33

8. User LEDs (Active-High)

Twenty active-High LEDs, shown in Table 9 and Table 10, page 17, are connected to user I/O pins on the FPGA. These LEDs can be used to indicate status or for any other user-designated purpose.

Table 9: **User LED, Row 1 (Top)**

Label	Pin		
	ML421	ML423	ML424
DS11	AC9	AJ16	AK13
DS12	AD8	AG15	AP14
DS13	AD9	AF15	AN14
DS14	V6	AF14	AL14
DS15	U7	AE14	AM15
DS16	U9	AE13	AJ14

Table 9: **User LED, Row 1 (Top) *(Continued)***

Label	Pin		
	ML421	ML423	ML424
DS17	N4	AH7	AU7
DS18	M4	AH8	AU8
DS19	AB9	AJ15	AH12
DS20	P3	AK9	AR9

Table 10: **User LED, Row 2 (Bottom)**

Label	Pin		
	ML421	ML423	ML424
DS31	V4	AH9	AK9
DS29	U4	AJ9	AL9
DS28	T3	AD9	AN9
DS32	T4	AD10	AP9
DS33	V8	AF13	AK14
DS34	R5	AM7	AR8
DS35	P5	AM8	AT8
DS8	AC3	AK11	AU11
DS9	AC4	AJ11	AT11
DS10	AC8	AK16	AK12

9. User DIP Switches (Active-High)

There are 20 active-High DIP switches, as shown in Table 11 and Table 12, page 18, connected to user I/O pins on the FPGA. These pins can be used to set control pins or any other purpose the user designates.

Table 11: **User DIP Switches, Row 1 (Top)**

SW5	Pin		
	ML421	ML423	ML424
1	L3	AJ7	AP7
2	AB6	AH15	AJ12
3	AB4	AE11	AP15
4	AB5	AD11	AN15

Table 11: **User DIP Switches, Row 1 (Top) *(Continued)***

SW5	Pin		
	ML421	ML423	ML424
5	AD3	AE9	AM11
6	AD4	AM12	AR12
7	U5	AM13	AP12
8	U6	AH12	AT13
9	AA8	AF9	AL11
10	AA9	AG11	AR13

Table 12: **User DIP Switches, Row 2 (Bottom)**

SW6	Pin		
	ML421	ML423	ML424
1	N3	AL9	AT9
2	Y8	AK7	AR7
3	Y7	AB12	AU16
4	T9	AA13	AU17
5	AA7	AL14	AU12
6	T8	AK14	AU13
7	AC11	AG12	AT14
8	AB11	AF11	AR14
9	AB7	AC12	AT16
10	L4	AB13	AT18

10. User Pushbutton Switches (Active-High)

Four active-High pushbutton switches, shown in Table 13, are connected to user I/O pins on the FPGA. These switches can be used for any purpose that the user designates.

Table 13: **User Pushbutton Switches**

Label	Pin		
	ML421	ML423	ML424
SW7	Y3	AH10	AP10
SW3	W4	AJ10	AN10
SW2	AA4	AF10	AJ10
SW1	AA3	AG10	AJ9

11. Xilinx Generic Interface

The XGI is an expansion interface for plug-in modules (for example, the SuperClock module) and provides the user access to the I/O pins listed in Table 14, Table 15, page 20, and Table 16, page 21. Table 17, page 21 shows header J10 with all pins connected to V_{CCO} for powering modules tied to this connector.

Table 14: **XGI Header (J13)**

Pin Number	ML421	ML423	ML424
1	U19	AC23	AU25
3	T18	AC22	AT25
5	AA17	AE22	AR27
7	Y17	AD22	AP27
9	AA20	AF25	AN30
11	AA19	AF24	AP30
13	AB22	AG25	AL30
15	AB21	AH25	AM30
17	AC21	AJ24	AM28
19	AD21	AH24	AL28
21	AB20	AL24	AN28
23	AB19	AK24	AN27
25	AC19	AK23	AK27
27	AC18	AK22	AL26
29	AB17	AH23	AU28
31	AB16	AG23	AU27
33	AA24	AE28	AM32
35	AA23	AF28	AN32
37	AB24	AH27	AT31
39	AC24	AJ27	AU31
41	AD24	AJ26	AK29
43	AD23	AJ25	AL29
45	AC23	AL26	AT30
47	AC22	AM26	AU30
49	AD20	AL25	AR29
51	AD19	AM25	AT29
53	AD18	AM23	AM27
55	AC17	AL23	AM26

Table 14: **XGI Header (J13) *(Continued)***

Pin Number	ML421	ML423	ML424
57	AD16	AM22	AR26
59	AC16	AM21	AP26
61	AB15	AL19	AT24
63	AA15	AL18	AR24

The pin order in Table 15 is arranged from top to bottom as viewed on the board. It does not reflect the physical connection to this connector.

Table 15: **XGI Header (J11)**

Pin Number	ML421	ML423	ML424
1	IIC	IIC	IIC
2	IIC	IIC	IIC
3	U24	AG18	AP35
4	T24	AF18	AP34
5	Y16	AG16	AU26
6	Y15	AG17	AT26
7	W24	AF19	AT35
8	V24	AE17	AU35
9	AF14	AF21	AN20
10	AF13	AE21	AP20
11	AD15	AE16	AM22
12	AD14	AF16	AN22
13	AD13	AK29	AL19
14	AC14	AJ29	AL21
15	AC13	AK21	AK19
16	AC12	AL21	AJ19
17	AB12	AL29	AM21
18	AA12	AM30	AM20
19	TDO	TDO	TDO
20	X TDO	X TDO	X TDO
21	TCK	TCK	TCK
22	TMS	TMS	TMS
23	NC	NC	NC
24	VCC3	VCC3	VCC3
25	VCC3	VCC3	VCC3

Table 15: **XGI Header (J11) *(Continued)***

Pin Number	ML421	ML423	ML424
26	VCC3	VCC3	VCC3
27	VCC3	VCC3	VCC3
28	NC	NC	NC
29	VCC5	VCC5	VCC5
30	VCC5	VCC5	VCC5
31	VCC5	VCC5	VCC5
32	VCC5	VCC5	VCC5

Table 16: **XGI Header (J10)**

Pin Number	ML421	ML423	ML424
1 - 32	VCCO	VCCO	VCCO

The pin order in Table 17 is arranged from top to bottom as viewed on the board. It does not reflect the physical connection to this connector.

Table 17: **XGI Header (J14)**

Pin Number	ML421	ML423	ML424
2	E20	G22	J27
4	D20	H22	K27
6	E22	C24	J29
8	E21	D24	H29
10	C23	E26	D30
12	C22	D26	C30
14	D24	C28	L31
16	C24	C27	L30
18	E23	F28	E32
20	D23	E28	D32
22	F24	G26	G30
24	F23	F26	F30
26	H22	J25	E29
28	G22	H25	F29
30	K22	L26	F33
32	L23	L25	E33
34	K21	E24	K29

Table 17: **XGI Header (J14) *(Continued)***

Pin Number	ML421	ML423	ML424
36	J21	F24	L29
38	G21	D25	J30
40	F22	C25	H30
42	H24	E27	E31
44	G24	D27	D31
46	J23	G25	D29
48	K23	F25	C29
50	L24	K26	G31
52	M24	J26	F31
54	N24	K24	G33
56	N23	L24	G32
58	M22	P24	C33
60	N22	N24	C32
62	K20	J22	D27
64	L19	K22	E27

12. LVDS Header Interface

The LVDS header interface allows the user to experiment with the LVDS I/O pairs as shown in Table 18, page 22 and Table 19, page 24. These I/O pins can also be used for any purpose designated by the user.

Table 18: **LVDS Header (J139)**

Pin Number	ML421	ML423	ML424
2		D16	D14
4		D15	C14
6		C13	K13
8		C12	J12
10		D12	D11
12		D11	E11
14		C9	E9
16		C8	F9
18		D6	C5
20		C5	D5
22		G10	C10

Table 18: **LVDS Header (J139) *(Continued)***

Pin Number	ML421	ML423	ML424
24		H10	D10
26		G7	E8
28		H7	F8
30		M12	E3
32		M11	F3
34		AB11	AH14
36		AA11	AH13
38		AD12	AT15
40		AE12	AU15
42		AG13	AL13
44		AH13	AM13
46		AL8	AN8
48		AK8	AN7
50		AL10	AU10
52		AM10	AT10
54		AJ12	AP11
56		AK12	AR11
58		AK13	AK11
60		AL13	AJ11
62		AD14	AP16
64		AC13	AR16

Table 19: **LVDS Header (J101)**

Pin Number	ML421	ML423	ML424
1		C29	C34
3		D29	D34
5		D31	J32
7		E31	K32
9		F31	F35
1		E32	G35
13		G31	F36
15		G32	G36
17		J29	H35
19		K29	J35
21		M25	K33
23		M26	L33
25		N32	T29
27		P32	T30
29		U27	V27
31		U28	W27

Note: All remaining I/O pins are connected to external capacitors for I/O load testing.

13. Program Switch (Active-Low)

The active-Low program switch, when pressed, grounds the program pin of the FPGA.

14. Reset Switch (Active-Low)

The active-Low reset switch resets the System ACE controller.

15. DONE LED

The DONE LED indicates the status of the DONE pin of the FPGA. This LED lights when DONE is High, indicating the FPGA is programed or that power is applied to the board without a part in the socket.

16. INIT LED

The INIT LED lights during initialization.

17. System ACE Controller

An onboard System ACE controller allows the user to store multiple configuration files on a CompactFlash memory card. These configuration files can be used to program the FPGA.

18. Configuration Address DIP Switch

This switch is used to select one of eight addresses in the CompactFlash memory card, from which a configuration bitstream can be read. The open (O) position indicates a Logic 0, and the closed (C) position indicates a Logic 1 as shown in Table 20.

Table 20: **Bitstream Address Table**

Address	2	1	0
0	O	O	O
1	O	O	C
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

19. RocketIO Transceiver Pins

All RocketIO transceiver pins are connected to differential SMA pairs. The RocketIO transceiver pins are shown in Table 21 (which spans multiple pages).

Table 21: **RocketIO Transceiver Pins**

Label	RocketIO Pin Name	V4FX20	V4FX40	V4FX60	V4FX100	V4FX140	ML421	ML423	ML424
J134	TXN_101A				X0Y9	X0Y11		A24	A25
J133	TXP_101A							A23	A24
J132	RXN_101A							A21	A22
J131	RXP_101A							A20	A21
J138	RXN_101B				X0Y8	X0Y10		A29	A30
J137	RXP_101B							A28	A29
J136	TXN_101B							A26	A27
J135	TXP_101B							A25	A26
J72	TXN_102A	X0Y3	X0Y5	X0Y7	X0Y7	X0Y9	A23	E34	A35
J66	TXP_102A						A22	D34	A34
J68	RXN_102A						A20	A32	A32
J67	RXP_102A						A19	A31	A31

Table 21: **RocketIO Transceiver Pins *(Continued)***

Label	RocketIO Pin Name	V4FX20	V4FX40	V4FX60	V4FX100	V4FX140	ML421	ML423	ML424
J65	RXN_102B	X0Y2	X0Y4	X0Y6	X0Y6	X0Y8	D26	K34	D39
J73	RXP_102B						C26	J34	C39
J70	TXN_102B						A25	G34	A37
J69	TXP_102B						A24	F34	A36
J86	TXN_103A		X0Y3	X0Y5	X0Y5	X0Y7	N26	W34	N39
J75	TXP_103A						M26	V34	M39
J78	RXN_103A						K26	T34	K39
J77	RXP_103A						J26	R34	J39
J74	RXN_103B		X0Y2	X0Y4	X0Y4	X0Y6	V26	AD34	V39
J87	RXP_103B						U26	AC34	U39
J85	TXN_103B						R26	AA34	R39
J84	TXP_103B						P26	Y34	P39
J154	TXN_104A					X0Y5			AD39
J149	TXP_104A								AC39
J155	RXN_104A								AA39
J148	RXP_104A								Y39
J152	RXN_104B					X0Y4			AJ39
J151	RXP_104B								AH39
J153	TXN_104B								AF39
J150	TXP_104B								AE39
J94	TXN_105A	X0Y1	X0Y1	X0Y3	X0Y3	X0Y3	AC26	AK34	AR39
J89	TXP_105A						AB26	AJ34	AP39
J91	RXN_105A						Y26	AG34	AM39
J90	RXP_105A						W26	AF34	AL39
J88	RXN_105B	X0Y0	X0Y0	X0Y2	X0Y2	X0Y2	AF23	AP31	AW36
J95	RXP_105B						AF24	AP32	AW37
J93	TXN_105B						AE26	AM34	AU39
J92	TXP_105B						AD26	AL34	AT39
J129	TXN_106A			X0Y1	X0Y1	X0Y1		AP22	AW27
J124	TXP_106A							AP23	AW28
J130	RXN_106A							AP25	AW30
J123	RXP_106A							AP26	AW31

Table 21: **RocketIO Transceiver Pins *(Continued)***

Label	RocketIO Pin Name	V4FX20	V4FX40	V4FX60	V4FX100	V4FX140	ML421	ML423	ML424
J127	RXN_106B			X0Y0	X0Y0	X0Y0		AP17	AW21
J126	RXP_106B							AP18	AW22
J128	TXN_106B							AP20	AW24
J125	TXP_106B							AP21	AW25
J110	TXN_109A			X1Y1	X1Y1	X1Y1		AP10	AW13
J109	TXP_109A							AP9	AW12
J108	RXN_109A							AP7	AW10
J107	RXP_109A							AP6	AW9
J114	RXN_109B			X1Y0	X1Y0	X1Y0		AP15	AW19
J113	RXP_109B							AP14	AW18
J112	TXN_109B							AP12	AW16
J111	TXP_109B							AP11	AW15
J47	TXN_110A	X1Y1	X1Y1	X1Y3	X1Y3	X1Y3	AF3	AG1	AR1
J42	TXP_110A						AF2	AF1	AP1
J44	RXN_110A						AD1	AD1	AM1
J43	RXP_110A						AC1	AC1	AL1
J41	RXN_110B	X1Y0	X1Y0	X1Y2	X1Y2	X1Y2	AF8	AM1	AW4
J48	RXP_110B						AF7	AL1	AW3
J46	TXN_110B						AF5	AJ1	AU1
J45	TXP_110B						AF4	AH1	AT1
J143	TXN_111A					X1Y5			AD1
J142	TXP_111A								AC1
J141	RXN_111A								AA1
J140	RXP_111A								Y1
J147	RXN_111B					X1Y4			AJ1
J146	RXP_111B								AH1
J145	TXN_111B								AF1
J144	TXP_111B								AE1
J31	TXN_112A		X1Y3	X1Y5	X1Y5	X1Y7	U1	T1	N1
J32	TXP_112A						T1	R1	M1
J30	RXN_112A						P1	N1	K1
J29	RXP_112A						N1	M1	J1

Table 21: **RocketIO Transceiver Pins *(Continued)***

Label	RocketIO Pin Name	V4FX20	V4FX40	V4FX60	V4FX100	V4FX140	ML421	ML423	ML424
J35	RXN_112B		X1Y2	X1Y4	X1Y4	X1Y6	AB1	AA1	V1
J38	RXP_112B						AA1	Y1	U1
J40	TXN_112B						W1	V1	R1
J39	TXP_112B						V1	U1	P1
J57	TXN_113A	X1Y3	X1Y5	X1Y7	X1Y7	X1Y9	C1	A3	A5
J50	TXP_113A						B1	A4	A6
J54	RXN_113A						A3	A6	A8
J53	RXP_113A						A4	A7	A9
J49	RXN_113B	X1Y2	X1Y4	X1Y6	X1Y6	X1Y8	H1	G1	D1
J59	RXP_113B						G1	F1	C1
J56	TXN_113B						E1	D1	A3
J55	TXP_113B						D1	C1	A4
J118	TXN_114A				X1Y9	X1Y11		A14	A15
J117	TXP_114A							A15	A16
J115	RXN_114A							A17	A18
J116	RXP_114A							A18	A19
J122	RXN_114B				X1Y8	X1Y10		A9	A10
J121	RXP_114B							A10	A11
J120	TXN_114B							A12	A13
J119	TXP_114B							A13	A14

20. RS-232 Port

The RS-232 port pins are as shown in Table 22. The pins are set up in DTE mode as shown in Figure 3.

Table 22: **RS-232 Port Pins**

FPGA UART Port Name	Direction	Port Name	ML421	ML423	ML424
TXD	OUT	T1IN	G16	E16	M25
RTS	OUT	T2IN	G15	F16	N24
CTS	IN	R2OUT	H11	F13	G15
RXD	IN	R1OUT	J11	G13	H15

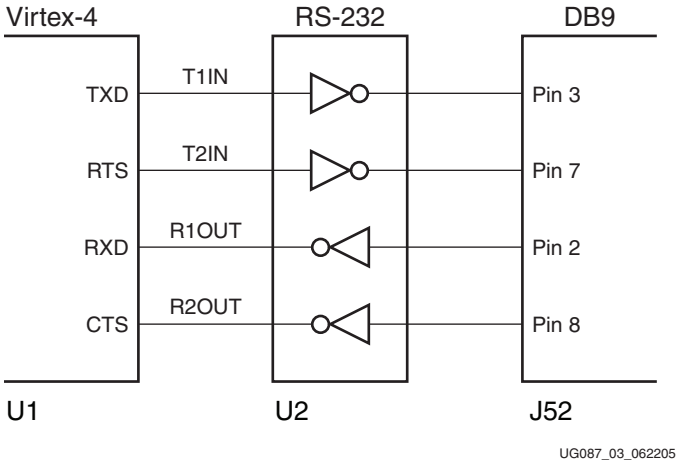


Figure 3: **RS-232 Pins in DTE Mode**

21. External Bias Potentiometers (RTERM)

Each Virtex-4 FPGA MGT column has two external pins that can be used to control internal bias currents and voltages in the analog section of the MGT known as the PMA (Physical Media Attachment). The external bias potentiometers are labeled RTERM 105 and RTERM 110. Through a master/slave bias circuit, these externally controlled biases can be shared across all MGT tiles within the MGT column. For more information on Rocket IO external biasing, see the *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* [Ref 1].

22. System ACE MPU Port

The 8-bit MPU port of the System ACE controller implemented on the ML52x series boards and the port connection to the DUT are shown in Table 23. For more information on the System ACE MPU port see *System ACE CompactFlash Solution [Ref 3]*.

Table 23: **System ACE Port Connections**

Pin Name	ML421	ML423	ML424
MPA00	H14	G17	K24
MPA01	G14	G16	J24
MPA02	H13	G15	L16
MPA03	H12	H15	M16
MPA04	D13	J16	G20
MPA05	E13	J15	F20
MPA06	C13	J14	F19
MPD00	J16	E18	H24
MPD01	H16	E17	H23
MPD02	K12	F15	J16
MPD03	K11	F14	K16
MPD04	F15	H17	J20
MPD05	E15	J17	J19
MPD06	D15	K18	H20
MPD07	D14	K17	H19
MPIRQ	J15	G18	L24
MPBRDY	J14	F18	K23
MPCE#	C12	K14	F18
MPOE#	J13	H13	E17
MPWE#	K13	H14	D17
CLK	A12	H19	K21

References

1. UG076, *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide*
2. UG070, *Virtex-4 FPGA User Guide*
3. DS080, *System ACE CompactFlash Solution*
4. UG091, *Xilinx Generic Interface (XGI) SuperClock Module User Guide*